## REMARKS/ARGUMENTS

Claims 1-26 are pending. Claims 1 and 19 and the specification have been amended to correct minor informalities. No new matter has been introduced. Applicants believe the claims comply with 35 U.S.C. § 112.

Section 112 Rejections

The Examiner objects to the specification under 35 U.S.C. § 112, first paragraph. The Examiner alleges that the specification is replete with terms which are not clear, concise, and exact. The Examiner objects to claim 1 for reciting that the sensitive silicon oxide layer has a wet etch rate of greater than about 6000 Å/min, because both the porous silicon oxide layer and the surface sensitive silicon oxide layer have a wet etch rate of greater than about 6000 Å/min.

Applicants note that the confusion apparently stems from the previous amendment to claim 1, which has now been amended to more particularly point out and distinctly claim Applicants' invention. Claim 1 as amended now recites that the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min. This is the definition of a surface sensitive silicon oxide layer on which the porous silicon oxide layer is formed. As discussed in the specification at page 17, lines 13-18, a surface sensitive silicon oxide layer, in the context of the present invention, is interpreted to mean a silicon oxide underlayer having physical characteristics such that a subsequent silicon oxide layer formed on the surface sensitive silicon oxide layer has a wet tech rate of greater than about 6000 Å/min. In claim 1, the subsequent silicon oxide layer is the porous silicon oxide layer.

Regarding claim 10, Applicants note that a plasma enhanced CVD silicon oxide layer is different from a thermal CVD silicon oxide layer. Claim 10 also recites that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.

Regarding claim 25, the specification at page 15, lines 15-20 discloses forming a surface sensitive barrier layer (step 500), and then a porous gap fill layer over the barrier layer (step 510), as shown in Fig. 5. The surface sensitive barrier only fills the gap partially, and the porous gap fill layer is formed over the barrier layer.

Accordingly, Applicants respectfully request withdrawal of the objections and rejections under 35 U.S.C. § 112.

Claims 1, 2, 4-7, 9, 23, and 24

Claims 1, 2, 4-7, 9, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho and Kwok et al.

Applicants respectfully submit that independent claim 1 is patentable over Cho and Kwok because, for instance, they do not disclose or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min, and the porous silicon oxide layer has a density of less than or equal to about 1.7 $g/cm^3$.

The Examiner alleges that Cho discloses a porous silicon oxide layer at column 5, lines 21-25. Applicants note, however, that Cho merely discloses that the mass density of $O_3$ is 70 to 130 $g/m^3$, but is devoid of any teaching of a silicon oxide layer density of less than or equal to about 1.7 $g/cm^3$.

The Examiner further alleges that it would have been obvious, in view of Kwok, to form a porous silicon oxide layer having a wet etch rate of greater than about 6000 Å/min. As pointed out in the specification at page 17, lines 8-12, Kwok discloses using various plasma treatments to the thermal oxide and PE-TEOS underlayers to reduce the surface sensitivity (see Kwok at page 2177). Thus, Kwok **teaches away** from forming a surface sensitive silicon oxide layer. It would not be obvious to form a porous silicon oxide layer having a wet etch rate of greater than about 6000 Å/min in view of Cho and Kwok.

As to claim 2, the Examiner alleges that it is inherent that an insulating film formed by a carbon containing silane will contain a carbon content of at least 5 atomic percent. The Examiner has no basis for the assertion. Moreover, an inherent feature may be relied upon to establish a rejection under 35 U.S.C. § 103(a), but only if such inherency would have been obvious to one of ordinary skill in the art. "That which may be inherent is not necessarily known." *In re Spormann*, 150 U.S.P.Q. 449, 452 (C.C.P.A. 1966). "Obviousness cannot be predicated on what is unknown." *Id.* In this case, the Examiner has not made a showing that

such inherency would have been obvious to one of ordinary skill in the art. Indeed, the references are completely silent as to the carbon content.

As to claims 23 and 24, the Examiner alleges that Cho discloses that the silicon oxide layer (3) partially fills the at least one gap and the layer (4) filling the at least one gap. This clearly contradicts Fig. 1A of Cho which shows that the layer (3) completely fills the at least one gap and that the layer (4) is not a gap-filling layer at all.

For at least the foregoing reasons, claim 1 and claims 2, 4-7, 9, 23, and 24 depending therefrom are patentable over Cho and Kwok et al.

Claims 3 and 8

Claims 3 and 8 depend from claim 1, and are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho and Kwok et al., in view of Lan.

The Examiner recognizes that neither Cho nor Kwok et al. discloses a porous silicon oxide layer having a dielectric constant of between about 2.9 and 3.2, and cites Lan for allegedly supplying the missing teaching. Lan, however, merely discloses a dielectric constant of 4.0-4.9. The Examiner's assertion that the porous silicon oxide layer would have a lower dielectric constant of between about 2.9 and 3.2 is based purely on conjecture with no support in the cited art. In addition, Lan does not cure the deficiencies of Cho and Kwok et al., in that Lan also fails to disclose or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the porous silicon oxide layer has a wet etch rate of greater than about 6000 Å/min, and the porous silicon oxide layer has a density of less than or equal to about 1.7 g/cm$^3$, as recited in claim 1 from which claims 3 and 8 depend. Therefore, claims 3 and 8 are patentable.

Claims 10-19, 21, and 22

Claims 10-19, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho and Kwok et al., in view of Lan.

Applicants respectfully assert that independent claim 10 is patentable over Cho, Kwok, and Lan because, for instance, they do not teach or suggest depositing a plasma enhanced CVD silicon oxide layer over a plurality of conductive lines, and depositing a thermal silicon oxide layer over the plasma enhanced CVD silicon oxide layer. These references also fail to

disclose or suggest that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.

The Examiner concedes that Cho fails to teach forming a plasma-enhanced CVD silicon oxide layer, but alleges that it would have been obvious to modify Cho in view of Kwok to form a plasma-enhanced CVD silicon oxide layer. Cho discloses varying TEOS flow rates while forming intermetallic insulating layers, and does not mention plasma at all. Kwok is directed to the study of surface related phenomena of $O_3$-TEOS SACVD films on different types of plasma-enhanced CVD oxides. Cho and Kwok relate to different processes and solve different problems. The references do not provide any teaching whereby the combination would have been obvious. Thus, Applicants believe the Examiner has engaged in the impermissible hindsight reconstruction of the claimed invention in this regard.

Furthermore, the cited references do not disclose or suggest that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent. As discussed above, Lan merely discloses a dielectric constant of 4.0-4.9. The Examiner's assertion that the porous silicon oxide layer would have a lower dielectric constant of between about 2.9 and 3.2 is based purely on conjecture with no support in the cited art.

The Examiner alleges that it is "inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS) contains a carbon content of at least 5 atomic %." This assertion is speculative and baseless. "Prior art SACVD $O_3$/TEOS layers generally have a carbon content of between 2-3 at.%. The porous SACVD $O_3$/TEOS layer of the present invention, however, has a significantly higher amount of carbon, at least 5 at.%, incorporated into the layer." Page 18, lines 30-33. As discussed above, an inherent feature may be relied upon to establish a rejection under 35 U.S.C. § 103(a), but only if such inherency would have been obvious to one of ordinary skill in the art. "That which may be inherent is not necessarily known." *In re Spormann*, 150 U.S.P.Q. 449, 452 (C.C.P.A. 1966). "Obviousness cannot be predicated on what is unknown." *Id.* In this case, the Examiner has not made a showing that such inherency would have been obvious to one of ordinary skill in the art. Indeed, the references are completely silent as to the carbon content.

Claims 11-19 and 21-22 depend from claim 10, and recite additional features not taught or suggested in the references. For example, claim 11 recites that the density of said thermal silicon oxide layer is less than or equal to about 1.7 $g/cm^3$. Claim 18 recites that the plasma enhanced and thermal CVD silicon oxide layers are deposited in an in situ process. Claim 21 recites that the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines. Claim 22 recites that the thermal silicon oxide layer fills the gaps between the plurality of conductive lines.

For at least the foregoing reasons, claim 10 and claims 11-19 and 21-22 depending therefrom are patentable over Cho, Kwok, and Lan.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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